REVIEW

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Tunnel field-effect transistors as energy-efficient electronic switches

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Power dissipation is a fundamental problem for nanoelectronic circuits. Scaling the supply voltage reduces the energy needed for switching, but the field-effect transistors (FETs) in today's integrated circuits require at least 60 mV of gate voltage to increase the current by one order of magnitude at room temperature. Tunnel FETs avoid this limit by using quantum-mechanical band-to-band tunnelling, rather than thermal injection, to inject charge carriers into the device channel. Tunnel FETs based on ultrathin semiconducting films or nanowires could achieve a 100-fold power reduction over complementary metal–oxide–semiconductor (CMOS) transistors, so integrating tunnel FETs with CMOS technology could improve low-power integrated circuits.

Reducing the size of complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs) has enabled extraordinary improvements in the switching speed, density, functionality and cost of microprocessors. But advanced CMOS technology now faces two problems[1] that together result in high power consumption: the increasing difficulty in further reducing the supply voltage, and stopping the rising leakage currents that degrade the switching ratio of 'on' and 'off' currents (I_{ON}/I_{OFF}). Recent reviews[2,3] have highlighted the need for new devices that can compete with or complement CMOS transistors.

Here we review the physics, design and optimization of one such device, the tunnel FET (TFET), and consider the potential and drawbacks of this energy-efficient device that could bring the voltage supply of integrated circuits below 0.5 V. We discuss the technology boosters needed to increase its performance, the reduced sensitivity of its direct current characteristics to gate length, and the variability of its electrical characteristics to changes in conditions. Finally, we compare its performance in various material systems — silicon, group III–V compounds and carbon — and discuss the related problems.

The quest for an energy-efficient switch

In a metal–oxide–semiconductor FET (MOSFET), the current-switching process involves the thermionic (temperature-dependent) injection of electrons[4,5] over an energy barrier. This sets a fundamental limit to the steepness of the transition slope from the off to the on state. The gate voltage required to change the drain current by one order of magnitude when the transistor is operated in the subthreshold region is reflected in the expression of the subthreshold swing, S:

$$S = \underbrace{\frac{dV_G}{d\Psi_S}}_{m}\underbrace{\frac{d\Psi_S}{d(\log_{10} I_D)}}_{n} \cong \left(1+\frac{C_d}{C_{ox}}\right)\ln 10\frac{kT}{q} \rightarrow \frac{kT}{q}\ln 10 \cong 60\ \text{mV decade}^{-1}\,|\,T = 300\ \text{K} \quad (1)$$

where V_G is the gate voltage, I_D is the drain current, kT/q is the thermal voltage, and C_d and C_{ox} are the depletion and the oxide capacitances, respectively. The term m is the transistor body factor, and n is a factor that characterizes the change of the drain current with the surface potential, Ψ_S, reflecting the conduction mechanism in the channel. A subthermal S would be less than kT/q ln10 and could be obtained by using new physical principles rather than thermionic injection.

As the transistor gate length is reduced, improved performance requires the supply voltage, V_{DD}, and simultaneously the threshold voltage, V_T, to be lowered to keep the overdrive factor ($V_{DD} - V_T$) high. As a consequence, the leakage current, I_{OFF}, increases exponentially (see the vertical intercept of I–V plots in Fig. 1a) because the S of a MOSFET is not scalable but has a minimum value of 60 mV per decade (that is, it takes 60 mV to increase the current by one order of magnitude) at room temperature. Typical values of S in advanced CMOS technology are close to 100 mV per decade; by lowering V_{DD} from 500 mV to 250 mV while preserving the overdrive, the leakage power has been shown to increase unacceptably by a factor of 275 in a 45-nm bulk CMOS technology[6].

Another way of reducing the voltage supply without performance loss is to increase the turn-on steepness, which means decreasing the average subthreshold swing, S_{avg}[7,8], defined as:

$$S_{avg} = \frac{V_T - V_{GOFF}}{\log\frac{I_T}{I_{OFF}}} \approx \frac{V_{DD}}{\log\frac{I_{ON}}{I_{OFF}}} \quad (2)$$

Therefore, devices with a steep S, called steep-slope switches, are expected to enable V_{DD} scaling.

Figure 1b shows a qualitative comparison of some major candidates to improve the characteristics of bulk silicon MOSFET switches: multigate devices for improved electrostatics; high-mobility channels exploiting group III–V and SiGe materials; and TFETs that use quantum-mechanical tunnelling. At moderate performance requirements, such as operation point A, TFETs offer not only improved I_{ON}/I_{OFF}, but also superior performance (higher I_{ON} at the same voltage) or power savings at the same performance (lower voltage for the same I_{ON}) over MOSFETs. However, when a much higher performance is required, such as at operation point B, a MOSFET is the better solution.

The energy efficiency of a logic operation can be evaluated by analysing its switching energy diagram[9,10] (Fig. 1c), showing the balance of the dynamic, $E_{dynamic}$, and the leakage, $E_{leakage}$, components of the total switching energy, E, versus the V_{DD}:

$$\begin{aligned} E_{total} &= E_{dynamic} + E_{leakage} = \alpha L_d C V_{DD}^2 + L_d I_{OFF} V_{DD} \tau_{delay} \\ &\approx \alpha L_d C V_{DD}^2 = L_d C V_{DD}^2 \frac{I_{OFF}}{I_{ON}} = L_d C V_{DD}^2\left(\alpha + \frac{I_{OFF}}{I_{ON}}\right) \\ &\approx L_d C V_{DD}^2\left(\alpha + 10^{\frac{-V_{DD}}{S}}\right) \end{aligned} \quad (3)$$

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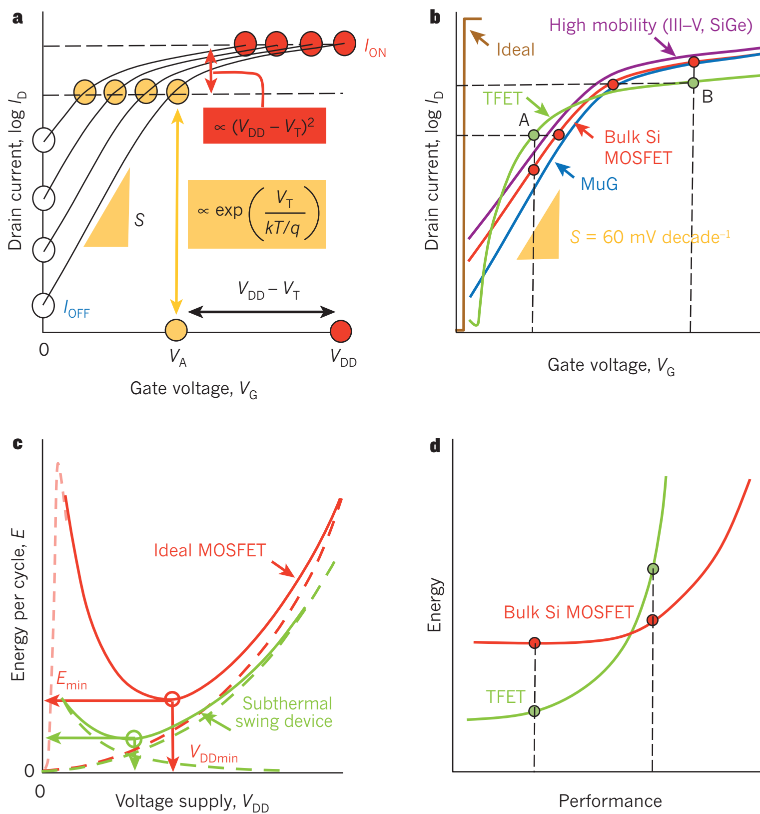

Figure 1 | Power challenge and main characteristics of an energy-efficient tunnel FET. a, Transfer characteristics (drain current, I_D, and gate voltage, V_G) of a MOSFET switch showing an exponential increase in I_{OFF} (more than tenfold increase for every 60 mV at room temperature) because of an incompressible subthreshold swing, *S*. Here the simultaneous scaling down of both the supply voltage, V_{DD}, and the threshold voltage, V_T, maintains the same performance (I_{ON}) by keeping the overdrive ($V_{DD} - V_T$) constant. **b**, Qualitative comparison of three engineering solutions to improve the characteristics of the bulk silicon MOSFET switch (red): a multigate device (MuG, blue) for improved electrostatics; a high-mobility channel (purple) using group III–V and SiGe materials; and a TFET (green), which has a steep off–on transition and the lowest I_{OFF}. At operation point A, because of its subthermal subthreshold swing, the TFET offers not only an improved I_{ON}/I_{OFF} but also a superior performance and a power saving at the same performance as a MOSFET. At operation point B, corresponding to higher performance, the MOSFET switch becomes the better solution. **c**, Comparison of the minimum switching energy, E_{min}, and the corresponding voltage supply, V_{DDmin}, for a subthermal swing device ($S < 60$ mV decade^{-1}, green curve) and the ideal MOSFET ($S = 60$ mV decade^{-1}, red) at the same I_{ON}/I_{OFF}. **d**, Comparison between switching energy and performance for a MOSFET and a TFET. The steep-swing TFET offers better energy efficiency at lower or moderate performance level.

where L_d is the logic depth, *C* is the switched capacitance, τ_{delay} is the delay time and α is the logic activity factor (typically ~0.01). The operation frequency, *f*, can be expressed as

$$f = \frac{1}{L_d \tau_{delay}} \quad (4)$$

and in modern technologies can be considered empirically as being proportional to V_{DD} (ref. 11). Therefore the power dissipation, *P*, is

$$P = \alpha L_d C V_{DD}^2 f = I_{OFF} V_{DD} \approx KCV_{DD}^3 = I_{OFF} V_{DD}^3 \quad (5)$$

Consequently, a technology that would enable a fivefold voltage scaling (from 1.0 V to 0.2 V) with a negligible leakage power could offer a 125-fold power dissipation reduction. From equation (3), it seems that CMOS logic has a lower limit in energy per operation, E_{min}, owing to the exponential increase of the subthreshold leakage, I_{OFF}, with V_{DD} scaling (see Fig. 1c). Hanson *et al.*[10] showed that E_{min} is proportional to the switched capacitance multiplied by the square of the *S*, $C \times S^2$, whereas V_{DDmin} is proportional to *S*. Nose and Sakurai[12] demonstrated that for an optimized CMOS circuit design, the ratio of leakage to dynamic energy is approximately 0.3–0.5 across a wide range of parameters.

Equation (3) shows that at the same performance (I_{ON} and *f*), any device that can offer the required I_{ON}/I_{OFF} at a lower V_{DD} (based on a smaller *S*) will always be more energy efficient (lower E_{min} and V_{DDmin}). This is depicted in Fig. 1d, which compares the switching energy for a TFET and a MOSFET as a function of the performance required.

Many device innovations to lower *S* below the MOSFET thermal limit, by decreasing the factors *m* and *n* in equation (1), have been proposed. Reducing *n* to achieve a subthermal *S* involves a modification of the carrier-injection mechanism. For this, impact ionization[13] and quantum-mechanical band-to-band tunnelling (BTBT)[14] in TFETs have been proposed. Another alternative to decrease *S* is to reduce the body factor, *m*, to a value smaller than 1. This can be achieved by using the recently proposed negative-capacitance FET (NC-FET)[15–17] or micro- or nano-electromechanical (M/NEM) movable electrodes in M/NEM-FET or NEM relay devices[18–20], in which the instability points between the electrical and the mechanical force are used to define super-abrupt transitions between the off and on states. Experimentally, an *S* of less than 2 mV per decade has been demonstrated[18], but electromechanical devices have their own limitations, such as voltage-scaling limitations, reliability issues and a stringent need for a controlled environment for robust operation.

In this review, we concentrate on the TFET. The gated p-i-n structure, comprising a p- and an n-doped region on either side of a gated intrinsic region, was proposed in 1978 by Quinn *et al.*[21]. Banerjee *et al.*[22] studied the behaviour of a three-terminal silicon TFET, and Takeda *et al.*[23] explored various aspects specifically related to the scaling down. Baba[24] fabricated TFETs called surface tunnel transistors in group III–V materials. In 1995, Reddick and Amaratunga[25] reported experiments on silicon surface tunnel transistors. In 1996, Koga and Toriumi[26] proposed a three-terminal 'forward-biased' silicon tunnelling device as a post-CMOS switch candidate. In 2000, Hansch *et al.*[27] published experimental results on a reverse-biased vertical silicon TFET that had a highly doped boron delta-layer fabricated by molecular beam epitaxy. Aydin *et al.*[28] processed lateral TFETs on silicon-on-insulator (SOI) in 2004, which in principle were similar to TFETs without an intrinsic region. The gate over a p–n junction was intended to reduce the gate capacitance to increase the speed. Recently, TFETs fabricated in various material systems (carbon, silicon, SiGe and group III–V materials)[29–33] have emerged experimentally as the most promising candidates for switches with ultralow standby power and sub-0.5 V logic operation.

The physics of TFETs

In contrast to MOSFETs, in which charge carriers are thermally injected over a barrier, the primary injection mechanism in a TFET is interband tunnelling, whereby charge carriers transfer from one energy band into another at a heavily doped p^+–n^+ junction. This tunnelling mechanism was first identified by Zener[14] in 1934. In a TFET, interband tunnelling can be switched on and off abruptly by controlling the band bending in the channel region by means of the gate bias. This function can be realized in a reverse-biased p-i-n structure (Fig. 2a). In principle, the TFET

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is an ambipolar device, showing p-type behaviour with dominant hole conduction and n-type behaviour with dominant electron conduction.

However, by designing an asymmetry in the doping level or profile, or by restricting the movement of one type of charge carrier using heterostructures, the tunnelling barrier at the drain can be widened to suppress the ambipolarity[8,34]. The asymmetry also achieves a low off-state current[3]. In the TFET off state (dashed blue line in Fig. 2b), the valence band edge of the channel is located below the conduction band edge of the source, so BTBT is suppressed, leading to very small TFET off-state currents that are dictated by the reverse-biased p-i-n diode. Applying a negative gate voltage (solid red curve in Fig. 2b) pulls the energy bands up. A conductive channel opens as soon as the channel valence band has been lifted above the source conduction band because carriers can now tunnel into empty states of the channel. Because only carriers in the energy window $\Delta\Phi$ can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy part of the source Fermi distribution is effectively cut off[35], as shown in Fig. 2b. Thus the electronic system is effectively 'cooled down', acting as a conventional MOSFET at a lower temperature. This filtering function makes it possible to achieve an S of below 60 mV per decade (Fig. 2c). However, the channel valence band can be lifted by a small change in gate voltage, and the tunnelling width can effectively be reduced by the gate voltage[36,37]. As a consequence of the BTBT mechanism, S in a TFET is not constant, but depends on the applied gate–source bias, as indicated in Fig. 2c, increasing with the gate-to-source bias. The key to the better voltage scaling of a TFET than a MOSFET is that S remains below 60 mV per decade over several orders of magnitude of drain current.

One challenge in TFETs is to realize high on currents because I_{ON} critically depends on the transmission probability, T_{WKB}, of the interband tunnelling barrier. This barrier can be approximated by a triangular potential, as indicated by the grey shading in Fig. 2b, so T can be calculated using the Wentzel–Kramer–Brillouin (WKB) approximation[4,36]:

$$T_{\mathrm{WKB}} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\,3}}}{3q\hbar\,(E_g+\Delta\Phi)}\right) \qquad (6)$$

where m^* is the effective mass and E_g is the bandgap. Here, λ is the screening tunnelling length and describes the spatial extent of the transition region at the source–channel interface (Fig. 2b); it depends on the specific device geometry. In a TFET, at constant drain voltage, V_D, the V_G increase reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$), so that in a first approximation the drain current is a super-exponential function[37] of V_G. As a result, in contrast to the MOSFET, the point subthreshold swing of the TFET is no longer a constant but strongly depends on V_G. The smallest subthermal values occur at the lowest gate voltages. A high on current requires a high transparency of the tunnelling barrier, thus maximizing T_{WKB}, which in the best case should be unity. Equation (6) suggests optimized design approaches to boost the on current. Luisier and Klimeck[38] found that the WKB approximation works properly in direct bandgap semiconductors, such as InAs (if one single imaginary path connecting the valence band and the conduction band dominates the tunnelling process), but has limited accuracy for Si and Ge structures or when quantum effects and phonon-assisted tunnelling become dominant.

Fundamental performance boosters

The goals for TFET optimization are to simultaneously achieve the highest possible I_{ON}, the lowest S_{avg} over many orders of magnitude of drain current, and the lowest possible I_{OFF}. To outperform CMOS transistors, the target parameters for TFETs are: I_{ON} in the range of hundreds of milliamperes; S_{avg} far below 60 mV per decade for five decades of current; $I_{ON}/I_{OFF} > 10^5$; and $V_{DD} < 0.5$ V. Because S decreases with the V_G (Fig. 2c), TFETs are naturally optimized for low-voltage operation.

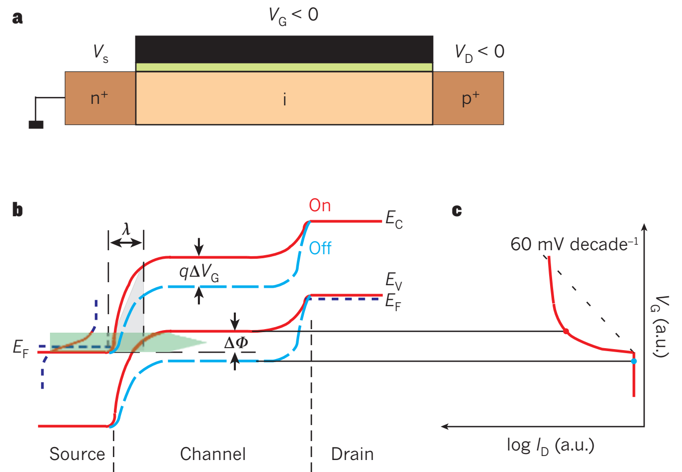

Figure 2 | Principle of operation of a TFET. **a**, Schematic cross-section of p-type TFET with applied source (V_S), gate (V_G) and drain (V_D) voltages. **b**, Schematic energy band profile for the off state (dashed blue lines) and the on state (red lines) in a p-type TFET. In the off state, no empty states are available in the channel for tunnelling from the source, so the off current is very low. Decreasing V_G moves the valence band energy (E_V) of the channel above the conduction band energy (E_C) of the source so that interband tunnelling can occur. This switches the device to the on state, in which electrons in the energy window, $\Delta\Phi$ (green shading), can tunnel from the source conduction band into the channel valence band. Electrons in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel at their energy (dotted black line), so a slope of less than 60 mV decade^{-1} can be achieved. This is indicated in the schematic transfer characteristics shown in **c**. In contrast to a conventional MOSFET, a TFET has a slope that is not linear on a logarithmic scale, which can be explained by the complex dependency of the tunnel current on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions. The BTBT can be approximated by the triangular potential barrier indicated in grey. Because the tunnel current depends on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions, the resultant slope is not linear on a logarithmic scale, which it is for a conventional MOSFET. λ, screening tunnelling length. a.u., arbitrary units; E_F, Fermi energy.

To realize a high tunnelling current and a steep slope, the transmission probability of the source tunnelling barrier should become close to unity for a small change in V_G. The WKB approximation, shown in equation (6), suggests that the bandgap (E_g), the effective carrier mass (m^*) and the screening tunnelling length (λ) should be minimized for high barrier transparency. Whereas E_g and m^* depend solely on the material system, λ is strongly influenced by several parameters, such as the device geometry, dimensions, doping profiles and gate capacitance[3,39,40]. A small λ results in a strong modulation of the channel bands by the gate. This requires a high-permittivity (high-κ) gate dielectric[8] with as low an equivalent oxide thickness as possible. Furthermore, the body thickness of the channel should be minimized, showing in the best case one-dimensional electronic transport behaviour[36,39]. The abruptness of the doping profile at the tunnel junction is also important. To minimize the tunnelling barrier, the high source doping level must fall off to the intrinsic channel in as short a width as possible. This requires a change in the doping concentration of about 4–5 orders of magnitude within a distance of only a few nanometres[40,41]. Increasing the source doping reduces λ and may lead to a slightly smaller energy barrier at the tunnel junction because of bandgap narrowing[40]. However, the energy filtering effect described above becomes effective only if the Fermi energy in the source is not too large[36].

TFETs do not follow the same scaling rules as MOSFETs, in which many parameters must be scaled simultaneously to keep the same electric field throughout the device[42]. In a TFET, the high electric fields exist only at the junctions. The current is determined by the screening

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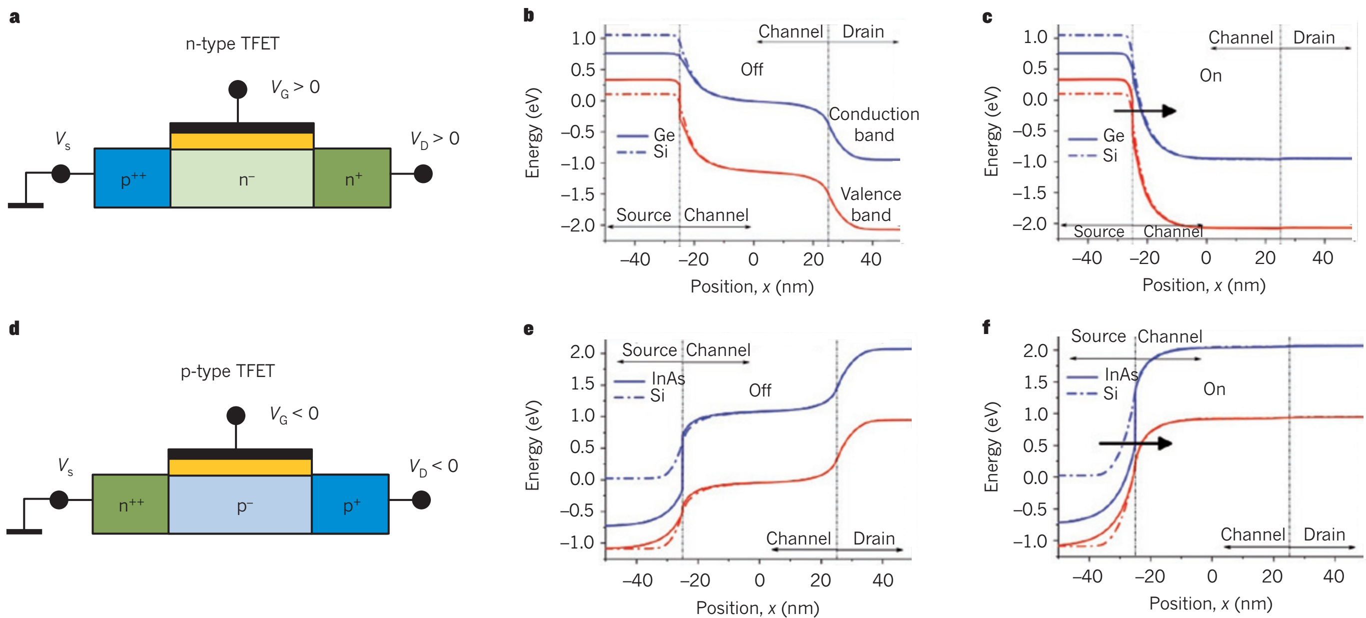


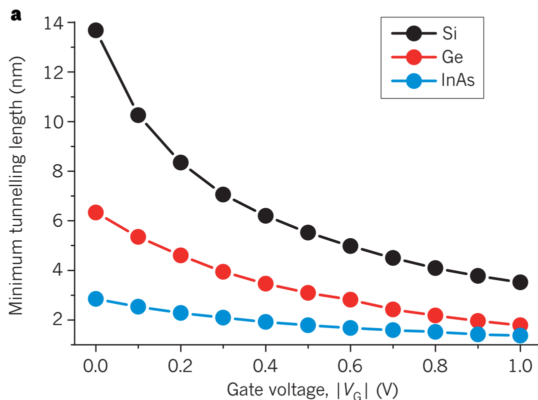
Figure 3 | Band diagrams of heterostructure C-TFETs. C- TFET device n-type (**a**–**c**) and p-type (**d**–**f**) architectures (**a**, **b**) and related band diagrams in the off (**b**, **e**) and on (**c**, **f**) state for two major implementations: all-silicon n- and p-type devices (dashed lines) and heterostructures with a Ge source and Si channel for the n-type switch and an InAs source and silicon channel for the p-type switch (solid lines). Band diagrams correspond to device architectures with a channel length of 50 nm and a high-κ dielectric thickness of 3 nm. The graphs show the conduction band (blue) and the valence band (red).

tunnelling length, so that the length of the intrinsic region has little effect on the device characteristics, as long as the length is above some critical length, L_{crit} (~20 nm for silicon TFETs[42]), at which p-i-n leakage becomes predominant. Experimental results[43] confirmed the lack of dependence of I_{ON} on TFET length.

Device optimization should apply to both n- and p-type TFETs simultaneously, to offer a complementary TFET (C-TFET) technology for logic circuits. In a heterostructure TFET, the materials are chosen such that the source material has a small bandgap, so that the width of the energy barrier at the source junction is reduced in the on state, whereas the drain material has a large bandgap, which creates the largest possible energy barrier width at the drain side in the off state to keep the off current low. The way in which the bands line up with each other at the heterojunction is also crucial[44,45]. Knoch[46] suggested that although a broken line-up yields the best I_{ON}, only $S \geq 60$ mV per decade is obtained; therefore, a combination of steep S and high I_{ON} can been achieved with moderate doping and a staggered band lineup ($S = 33$ mV per decade and an intrinsic cutoff frequency of 4.74 THz)[47]. Koswatta *et al.*[48] included electron–phonon scattering in the transport model and found the best TFET performance for a broken-gap heterojunction.

Another optimization criterion is maximizing the gate modulation of the tunnelling barrier width by an appropriate alignment of the tunnelling path with the direction of the electric field modulated by the gate. By overlapping the gate with the tunnelling region, or designing a source region covered with an epitaxial intrinsic channel layer under the top gate, I_{ON} can be improved by a factor of more than 10 and a low S_{avg} can be obtained[49–52].

The effect of a staggered bandgap at the TFET source-to-channel junction as a technology booster is shown in Fig. 3. The aim is to find a solution for an optimized C-TFET. The simulated devices have a silicon channel length of 50 nm, a 20-nm-thick film and asymmetric



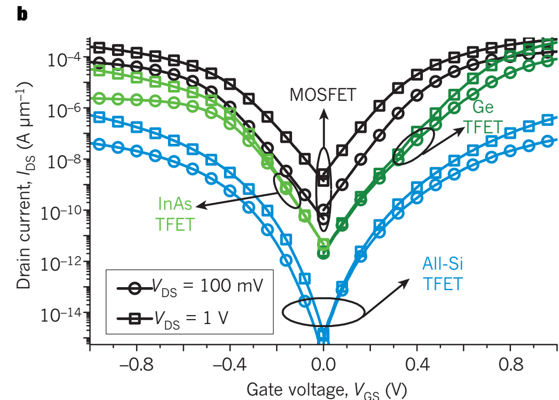


Figure 4 | Importance of the material system on TFET performance. a, Modulation of the minimum screening tunnelling length with the applied gate voltage in all-silicon (black), Ge-source (red) and InAs-source (blue) TFETs, showing the beneficial effect of a higher tunnelling rate due to the shorter tunnelling length in a heterostructure TFET with a low bandgap source material compared with silicon. By contrast, a higher ratio between the tunnelling length in the off and the on state reflects an improved I_{ON}/I_{OFF}. **b**, Corresponding transfer characteristics of a state-of-the-art 65-nm CMOS transistor (black), complementary Ge/InAs TFET (green) and complementary all-Si TFET (blue). The complementary Ge/InAs TFET achieves the best trade-off between a low I_{OFF}, a steep subthreshold swing and performance. I_{DS}, drain-to-source current; V_{DS}, drain-to-source voltage; V_{GS}, gate voltage at source.

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doping to avoid ambipolarity. The cross-section and bands in the off and the on state of the n-type TFET are shown in Fig. 3a–c. Changing the source material from Si to Ge considerably improves λ and $\Delta\Phi$ at the same applied V_G in the on state. A similar band-engineering optimization performed for the p-type device with an InAs source is shown in Fig. 3d–f. The corresponding reduction of the screening tunnelling length and its dependence on the V_G when the source bandgap is changed is depicted in Fig. 4a. The simulated I_D versus V_G characteristics of a 65-nm CMOS technology node with 50-nm all-Si C-TFETs and 50-nm Ge/InAs C-TFETs are compared in Fig. 4b. At $V_D = V_G = 1$ V, the Ge and InAs TFETs have on currents of 244 μA μm^{-1} and 83 mA mm^{-1}, respectively, which means improvements by factors of 480 and 162, respectively, over their all-Si TFET counterparts, and much lower I_{OFF} and I_{ON}/I_{OFF} than the 65-nm CMOS device. Their average swing over three decades of drain current is close to 60 mV per decade, showing that further optimization is needed. Heterostructure TFETs[33,45,46,53] similar to those reported here can offer viable solutions for on currents higher than 100 μA μm^{-1}, $I_{ON}/I_{OFF} > 10^7$ and V_{DD} smaller than 0.5 V. The all-Si C-TFETs have the lowest I_{OFF} and average subthreshold swings of less than 40 mV per decade, but their I_{ON} is not a good trade-off for performance compared with CMOS transistors.

Band-to-band tunnelling

The fundamental performance boosters of TFETs described before require engineering solutions concerning their design, choice of materials and integration with advanced silicon platforms. In this section we discuss existing and state-of-the-art research efforts aimed at TFET optimization, design and implementation, together with their experimental or predicted electrical performance.

All-silicon TFETs

TFETs offer the potential for a low off current and a small S, but they generally have a lower on current than conventional MOSFETs, so a smart design strategy could achieve a small S_{avg} and a high I_{ON} without degrading I_{OFF}. As with CMOS technology boosters, performance boosters for TFETs should not be suggested independently. Instead, an additive strategy of boosters for the same device should be applied, so that improvements in device performance are cumulative[54]. The major technology boosters for all-silicon TFETs include[54,55] the use of a high-κ gate dielectric, a more abrupt doping profile at the tunnel junction, a thinner body, higher source doping, a double gate, a gate oxide aligned with the intrinsic region, and a shorter intrinsic region (and gate) length.

The physics of TFETs are governed by the BTBT rate, so they differ from those of conventional MOSFETs. It is therefore likely that the sensitivity of the device's characteristics to variations in the technology parameters will differ too, which can imply new technology challenges. Boucart[56] predicted that TFET performance will be much less sensitive to doping fluctuations and gate length scaling than in conventional CMOS transistors. By contrast, control of the high-κ gate process, the abruptness of doping at the tunnel junction, and the film thickness in ultrathin-body SOI devices, with significantly less parameter variation than that required by CMOS devices, is crucial for building future TFETs with reproducible characteristics.

Figure 5a shows a recent all-silicon lateral TFET fabricated on fully depleted silicon with a silicon film thickness of 20 nm and a gate length of 100 nm[31,57] that benefits from some major technology boosters and from advanced engineering of the contacts. The device includes a high-κ gate stack (3 nm HfO_2, and 3 nm and 10 nm TiN), a double epitaxially raised Si source–drain, and an asymmetric n^+ source and p^+ drain achieved in two successive lithography and implantation steps. This all-silicon TFET shows extremely low I_{OFF} values (~10–100 fA μm^{-1}; Fig. 5b), but I_{ON} is less than 0.1 μA mm^{-1} at a V_{DD} of 1 V. By applying the same process and design to $Si_{1-x}Ge_xOI$ substrates (x = 0, 15% or 30%), extraordinary improvements in I_{ON} can be obtained[57]: a 335-fold improvement for the n-TFET and a 2,700-fold improvement for the p-TFET, compared with the SOI TFET counterparts (Fig. 5c). In recent

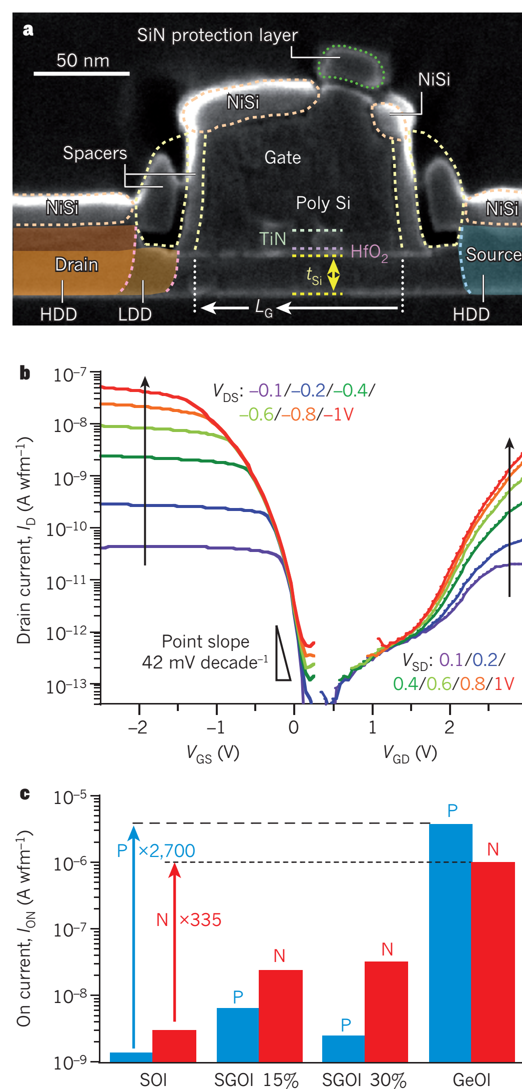

Figure 5 | Implementation of all-Si technology boosters. **a**, Scanning electron micrograph showing the cross-section of an SOI TFET from CEA-Leti that implemented some major technology boosters. Image reprinted, with permission, from ref. 31. **b**, I_D–V_G characteristics of the all-silicon TFET, showing a subthreshold swing at room temperature of 42 mV decade^{-1} and an I_{OFF} smaller than 100 fA μm^{-1} at V_{DS} = 1 V (different colours correspond to different values of V_D). **c**, A major improvement in I_{ON} obtained in an all-silicon C-TFET by applying the same design and fabrication of TFET on $Si_{1-x}Ge_xOI$ (molar fraction x = 0, 15% and 30%). Note the 335-fold and 2,700-fold improvements for the n-TFET (N) and p-TFET (P), respectively, for the SiGeOI over the SOI TFET. V_{DS}, drain-to-source voltage; V_{GD}, gate voltage at drain; V_{GS}, gate voltage at source; V_{SD}, source-to-drain voltage.

optimizations of an all-silicon TFET[58], values of I_{ON} close to 100 μA μm^{-1} in sub-60-nm devices were obtained.

Group III–V-semiconductor-based TFETs

A further strategy to improve I_{ON} and S is to use low-bandgap and low-effective-mass materials and band engineering to increase BTBT. For this, group III–V materials are very attractive as they can provide small tunnelling mass and allow different band-edge alignments.

Simulation showed that by reducing only the bandgap of the TFET material from Si to InAs or InSb, the I_{ON} increases by several orders of magnitude and can be reached at lower electric fields[3]. Recent experimental results for InGaAs TFETs indicate that a higher I_{ON} at a lower V_G than with Si TFETs seems possible[59,60]. The first InGaAs TFET by Mookerjea *et al.*[59] achieved an on current of 20 μA μm^{-1} with an S of

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250 mV per decade, whereas Zhao *et al.*[60] improved I_{ON} to 50 μA μm^{-1} with an S of around 90 mV per decade, which is the best local swing achieved so far for III–V-based TFETs but is still above the thermal limit of MOSFETs. The degraded S is attributed to parasitic tunnelling mechanisms involving traps in the source tunnel junction[61].

The effective bandgap for tunnelling can be decreased even further by using heterostructures. Although there is not yet full agreement on whether a staggered or a broken gap alignment works best, all theoretical studies predict that the TFET performance can be significantly enhanced compared with homojunctions[45–47,62]. The first experimental implementations of III–V heterojunction TFETs have only recently been demonstrated[63,64]. To reduce the tunnelling barrier, InAs and GaAsSb were chosen for the source, with AlGaSb and InGaAs for the channel. Another reason for selecting these materials is that they allow lattice-matched growth, and thus the use of conventional III–V growth and processing technologies.

For the C-TFET technology, the combination of an InAs source with a Si drain and channel yields the best on-state performance for the p-TFET[45]. However, InAs and Si possess a lattice mismatch of about 11%, which results in highly defective material growth and prevents integration onto Si in a conventional approach. This challenge can be met by using grown nanowires. They are attractive materials as they can be grown epitaxially via metal–organic chemical vapour deposition directly on Si(111) (refs 65, 66).

A comprehensive study has experimentally investigated[67] the quality and suitability of the InAs–Si heterojunction, which is a key element for high-performance TFETs. In particular, studying highly doped p–n junctions (so-called Esaki tunnel diodes) provides insight into the tunnel process, and thus the limits of the TFET drive can be explored. Figure 6a shows a schematic cross-section of such an InAs–Si heterostructure nanowire device in which the tunnel junction is located between the n-type InAs nanowire and the p-type Si substrate. The highest Si doping of 10^{20} atoms cm^{-3} produced tunnel diodes with current densities as high as 250 kA cm^{-2} at 0.5 V reverse bias (see Fig. 6c). The high tunnel currents and the observed negative differential resistance are indications of a well-defined and abrupt Si–InAs heterojunction[66].

Moreover, the vertical nanowire provides an optimal geometry for minimizing the screening tunnelling length, λ, by using a 'gate-all-around' (GAA) architecture, in which the gate is wrapped around the cylindrical nanowire channel to provide the best electrostatic control. Simulations have shown that λ is reduced three- to fourfold when using the GAA nanowire architecture compared with using a single-gate device with a channel thickness or diameter of 10 nm[68]. The cross-section of a recently fabricated vertical n-i-p InAs–Si–Si nanowire heterojunction TFET with InAs as a low-bandgap source[69] is shown in Fig. 6b. The single-nanowire TFET exhibits switching operation under reverse-bias conditions with an S of ~220 mV per decade and a drive current of ~0.4 μA μm^{-1} (see Fig. 6d). This first InAs-source, Si-channel TFET implementation needs further optimization. It is anticipated that the drive current can be improved by introducing n-type doping in the InAs wire, by scaling the equivalent oxide thickness, and by reducing the contact resistance.

Carbon-based TFETs

Carbon nanotubes and graphene nanoribbons are appealing materials for use in TFETs. The light effective mass of their charge carriers, their small and direct bandgap, and their excellent electrostatic control of the gate over the channel owing to the ultrathin body make them among the best choices in terms of both materials and device geometry. The first ever TFET demonstrating an S of less than 60 mV per decade was achieved with a carbon nanotube structure by Appenzeller *et al.*[29] in 2004. In their device, the electrostatics in the carbon nanotube were controlled by two independent gates. A common back gate electrostatically doped both the source and drain, and another gate allowed control of the channel bands, creating a p-i-p FET device. Although the on current was low because the carriers had to tunnel through two barriers, an S of 40 mV per decade was achieved for the first time. Furthermore, simulation and temperature-dependent measurements provided clear evidence that a carbon nanotube TFET had indeed been realized[29,35]. More advantageous would be the implementation of a p-i-n-structured carbon nanotube TFET. Progress has been hampered by the difficulty of establishing appropriately doped carbon nanotube regions and abrupt junctions. So far there has been little experimental verification of carbon nanotube TFETs, but several theoretical studies have been conducted[70]. The influence of electron–phonon scattering on the performance of carbon nanotube TFETs has also been investigated[71], and there is strong

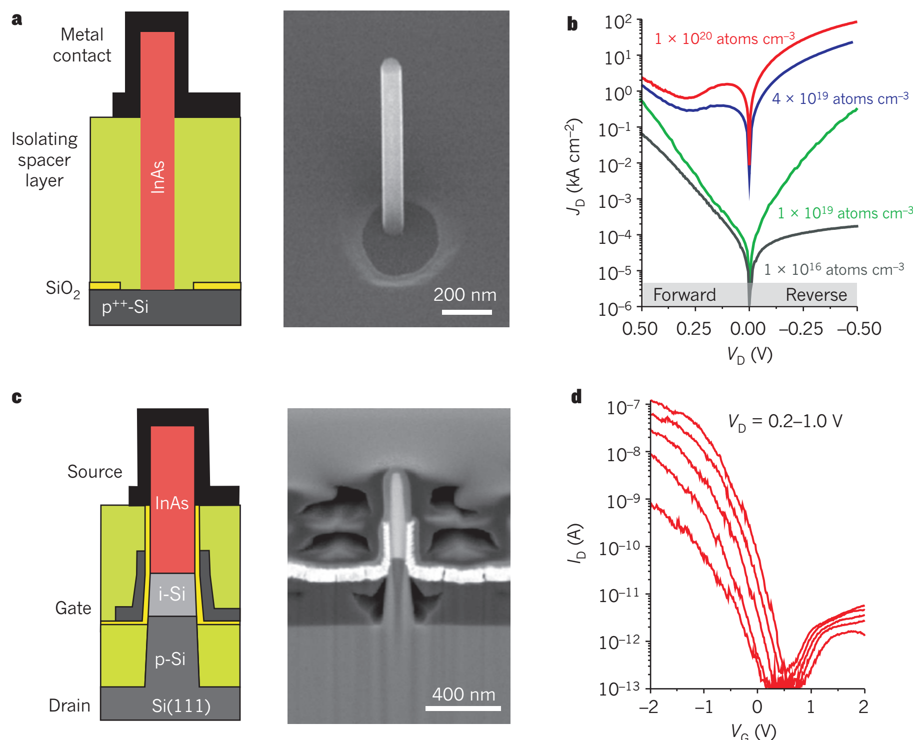

Figure 6 | InAs–Si heterojunction diodes and TFETs for improved performance. **a**, Left, schematic cross-section of an InAs–Si heterostructure nanowire diode. Right, scanning electron micrograph of an InAs nanowire grown epitaxially on Si. **b**, Current density–voltage (J_D–V) characteristics of Si–InAs heterojunction single-nanowire tunnel diodes. The high tunnel current densities required for TFETs are achieved for high doping levels. Different colours refer to different doping densities. **c**, Left, schematic cross-section of a vertical InAs–Si heterostructure nanowire TFET. Right, scanning electron micrograph showing a cross-section of the fabricated TFET. The InAs nanowire has a diameter of 100 nm, and the undoped Si channel on the p-type substrate is 150 nm long. **d**, Transfer characteristics, I_D–V_G, for various source–drain biases of the TFET shown in **c**.

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evidence that BTBT is dominated by optical phonon-assisted inelastic transport, which can lead to a degradation of the S.

Furthermore, simulations have shown that the specific energy dependence of the one-dimensional density of states (which arises because the nanowire radius is so small) can be exploited to reach the quantum capacitance limit, resulting in better control of the channel potential. In this regime, the quantum capacitance, C_q, which is determined by the change of the charge in the channel resulting from a change in gate potential, is far smaller than the oxide capacitance, C_{ox}, due to the BTBT, and thus almost equals the total capacitance. This leads to a reduced total capacitance and improves the gate delay[72].

TFETs based on graphene nanoribbons theoretically offer the same benefits as carbon nanotube TFETs and may also provide planar processing compatibility. But so far, only theoretical studies have been performed, and these demonstrate the high potential of graphene nanoribbons in significantly improving I_{ON} to several hundred μA μm^{-1}, with an I_{OFF} of only a few pA μm^{-1} and a slope of less than 20 mV per decade[73].

However, for a practical implementation using graphene nanoribbons, the influence of the line edge roughness on the bandgap and the transport properties, and thus on the TFET performance, must be considered. Luisier and Klimeck[74] found that with rougher edges, the off current significantly increases because of a lowering of the graphene nanoribbon bandgap and an increase in the source-to-drain tunnelling leakage through the gate potential barrier. This leads to a deterioration of S and I_{ON}/I_{OFF}, which are no longer sufficient and thus limit the switching performance of graphene nanoribbon TFETs. The theoretical investigations done so far show that graphene nanoribbon TFETs have great potential, although for a practical implementation, significant technical challenges need to be met. Fiori and Iannaccone[75] suggested using bilayer graphene to fabricate TFETs, presenting an attractive alternative to graphene nanoribbons. The benefit of this approach is that the required energy gap is opened by applying a vertical electric field to the graphene bilayer, rather than by preparing small ribbons, which would require single-atom precision patterning.

Energy-efficient integrated circuits

The 65-nm CMOS transistor and the 50-nm C-TFET in both silicon and Ge/InAs can be compared directly by simulating the main characteristics of inverter cells (the basic building blocks of a circuit) operating at the same V_{DD}. Figure 7a shows the voltage transfer characteristics of inverters in these three implementations. The Ge/InAs C-TFET inverter has the most abrupt transition between the 1 and 0 states because it has a steep slope combined with a reasonably high I_{ON}, which results in the best noise margins and the highest dV_{OUT}/dV_{IN} gain. However, the transient response of the Ge/InAs C-TFET inverter is worse than that of the CMOS at a V_{DD} of 1 V (or even 0.5 V) with an associated delay of 358 ps. The advantages of TFET logic should be explored at lower frequencies corresponding to low-power and low-standby-power CMOS specifications[76], especially in terms of power savings.

A specific characteristic of TFETs that influences their transient response was reported by Mookerjea *et al.*[77], who were the first to observe that in a TFET the gate capacitance, C_{GG}, is dominated by the gate-to-drain capacitance, C_{GD}, under all bias conditions. This is in strong contrast to a MOSFET, where the C_{GD} and the gate-to-source capacitance, C_{GS}, have relatively balanced contributions to the gate capacitance. In a TFET, C_{GD} predominates even near the off state because the source-to-channel barrier resistance is large and the channel-to-drain barrier resistance is low. Therefore, the effective load capacitance for unloaded TFET inverters can be more than twice the gate capacitance because of the enhanced Miller effect (an increase in the equivalent input capacitance of an inverting voltage amplifier resulting from the amplification of capacitance between the input and output terminals) and the effective drive current. This can degrade the delay time of TFET inverters and generate current overshoots.

In general, there is an agreement in all published studies that TFETs are attractive for low-standby-power applications. Koswatta *et al.*[78] proposed a performance comparison between p-i-n TFETs with a carbon nanotube channel and conventional thermionic silicon MOSFETs. Their choice of a carbon nanotube channel is motivated by its direct energy bandgap and small carrier mass. They based their study on a comprehensive simulation framework and on experimental results. Specifically, they investigated the delay time, τ, and the switching energy calculated as the power-delay product. They found the intrinsic delay to be similar for both devices, but the TFET became much slower when load capacitance was considered. They also reported that phonon scattering degrades τ for both devices, but this increase is more important for TFETs. When operated under the quantum capacitance limit, TFETs have smaller switching energies than MOSFETs.

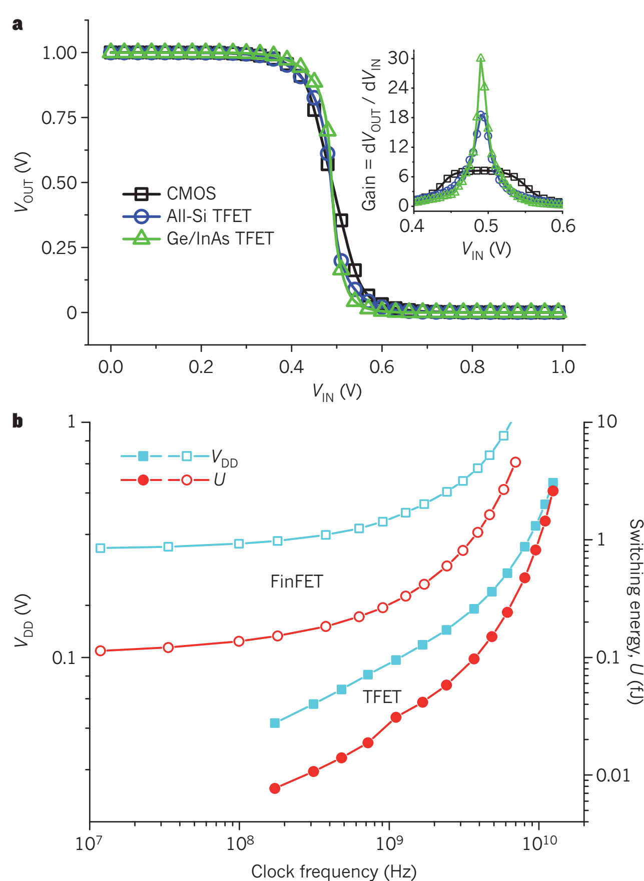

Figure 7 | Circuit-level characteristics of low-power TFETs. **a**, Comparison of the voltage transfer characteristics, V_{OUT}–V_{IN}, of CMOS and TFET inverters corresponding to the complementary device characteristics in Fig. 4b. The Ge/InAs C-TFET inverter has the most abrupt transition from the 1 to the 0 state with the highest differential gain, dV_{OUT}/dV_{IN} (inset) and best noise margins. **b**, Switching energy, U (red), and power supply voltage, V_{DD} (blue), against clock frequency simulated with a calibrated compact model for a heterostructure (In,Al)As/(Ga,Al)Sb TFET (filled symbols) and a silicon FinFET with a 20-nm channel length (open symbols); 16 cores of 1.5×10^6 circuits each are assumed. The total chip power was constrained, and V_{DD}, channel length, threshold voltage (V_T), Fermi energy level in the source (V_e), width and design were optimized to maximize the clock frequency[79]. Figure reprinted, with permission, from ref. 79.

Until recently, investigations of circuit performance have been limited by the lack of availability of accurate compact models for TFETs calibrated on fabricated n- and p-type TFETs. One way to circumvent this problem was to build look-up table (LUT) models for current–voltage and capacitance–voltage characteristics using simulation data. One such study[6] used a LUT model for a type II heterojunction tunnel transistor (HETT) and compared its power reduction with a commercial bulk CMOS 45-nm technology in simulated ring oscillators. At V_{DD} = 1 V, a high-performance CMOS ring oscillator has a period of 450 ps and

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53.9 μW dynamic power consumption, whereas the ring oscillator with a HETT consumes only 5.74 μW at 0.355 V to maintain the same period, achieving a 9.4-fold dynamic power reduction.

The most recent compact model for the TFET captures the essential physical features of the heterojunction TFET using the realistic case of (In,Al)As/(Ga,Al)Sb[79]. As well as the principal tunnelling mechanism, the effects of source degeneracy, back-injection from the drain, and direct source–drain tunnelling are included. Perhaps the most interesting idea of this study was to run the TFET model in an optimizer program that adjusts the device design parameters to achieve optimal chip-level performance when power and power density are constrained. The study compared 20-nm-channel-length TFET technology with FinFETs (multigate FET devices in which the gate is wrapped around a semiconducting channel shaped like a fin) in terms of switching energy and V_{DD} when the total chip power was constrained, and V_{DD} and the design parameters were varied to maximize the clock frequency (Fig. 7b). The calibrated simulations demonstrate the advantage of heterojunction TFETs over FinFETs in terms of both lower V_{DD} and switching energy.

In addition, TFETs retain their excellent switching characteristics even at high temperature[80–83] because the tunnelling mechanism makes them almost insensitive to temperature changes. Not only is the S invariable with temperature but so is the on current, which should increase only slightly owing to the decrease of the energy bandgap with temperature, as recently demonstrated experimentally[33,84].

Other attractive applications of TFETs are in analog integrated circuits[81] such as ultralow-power voltage-controlled oscillators and voltage references that have to deliver a well-defined output voltage, independently of supply voltage, temperature and process variations.

Finally, TFETs offer a solution for critical leakage power savings in static random access memory (SRAM). Six-transistor (6T)[85] and 4T[86] SRAM cell designs with CMOS and TFET technologies have been compared in terms of layout, performance and power on silicon platforms. A 700-fold improvement in leakage reduction over CMOS technology with a voltage supply of 0.3 V was demonstrated in the silicon TFET SRAM[85].

Conclusions

Today TFETs represent the most promising steep-slope switch candidate, having the potential to use a supply voltage significantly below 0.5 V and thereby offering significant power dissipation savings. Because of their low off currents, they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies (several hundred MHz). Other promising applications of TFETs include ultralow-power specialized analog integrated circuits with improved temperature stability and low-power SRAM.

The biggest challenge is to achieve high performance (high I_{ON}) without degrading I_{OFF}, combined with an S of less than 60 mV per decade over more than four decades of drain current. This requires the additive combination of the many technology boosters specific to complementary heterostructure TFETs, which are available or under research on advanced SOI CMOS platforms.

Carbon materials such as carbon nanotubes and graphene are well suited for use in high-performance TFETs because of their ultrathin body thickness and their one-dimensional transport characteristics. However, enormous challenges exist for the experimental implementation of carbon TFETs with all of the process parameters under control. Heterostructure TFETs offer the best performance compromise for complementary logic through advanced band engineering, using Ge and InAs sources on silicon platforms for n- and p-type TFETs in ultrathin films or nanowires (with $I_{ON}/I_{OFF} > 10^7$, $I_{ON} = 100\ \mu A\ \mu m^{-1}$ and $V_{DD} < 0.5$ V). Such TFETs could offer opportunities for a hybrid CMOS C-TFET design, with TFETs as an add-on ultralow-power device option on advanced CMOS platforms. ■

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